national accelerator laboratory

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WHAT MAKES THE BOOSTER LLRF TICK

J. Dinkel and E. Schmidt

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INTRODUCTION

It is the intention here to describe in as complete detail as possible, the components of the booster low-level RF (LLRF) system and how they are configured. We must keep in mind that it has two functions; to provide a frequency source for the booster high-level RF which tracks the particle velocity during acceleration, and to provide the necessary synchronization essential for a sequential batch-to-batch transfer into the main ring.

SYSTEM CONFIGURATION

There are two totally independent LLRF systems in the booster. The output of either system may be selected as the input to the high-level RF with a push-button transfer switch. Each LLRF system is composed of five circuit modules with two additional modules, common to both systems, that are required for synchronous injection into the main ring. The modules are interconnected as shown in Figure 1. The frequency source is a voltage controlled oscillator (VCO) programmed to an approximation of the ideal frequency with a digital waveform generator. Values of $\dot{F}$ and the times at which they occur are stored in a digital memory. When the memory cycle is initiated, the values are read into the reference source at the appropriate times and converted to a voltage approximation of the $\dot{F}$ curve. This voltage is integrated by a precision integrator which starts at a voltage level set by the F_0 D-A converter. The integrator remains clamped to the F_0 voltage level except during the acceleration cycle. An input is also included which permits fine tuning of the frequency by the feedback loops.

The VCO generates a second frequency program which sweeps 10 MHz above that used for acceleration and is used as a "local oscillator" in both radial and phase measuring systems. This allows these measuring systems to employ the superheterodyne principle to maintain a high signal-to-noise ratio inherent in a swept narrow band detector.

Radial position is measured at two points spaced such that the betatron phase advance is $(2N + 1)\pi$ with the amplitude function at each being the same. The transformer spacing prevents coupling of betatron motion and synchrotron motion through radial feedback. Transformers used for position measurement are a ferrite picture frame configuration with one coaxial turn on each side. Currents in both turns are compared both in phase and differentially to provide RF signals proportional to beam intensity and position. The sum and difference voltages from each transformer are detected and added to produce an average sum and difference as seen by the two transformers. These average values are then used by the normalizer to produce an intensity independent position signal.

The phase measuring system compares the instantaneous phase between the cavity gap voltage and beam current as seen by a pair of beam current transformers. Two transformers are used to make the system less susceptible to problems arising from missing bunches.

The phase detector is designed to provide a linear voltage-to-phase characteristic as shown in Figure 2. The beam is injected into stationary buckets at a phase angle which would be at the bottom tip of the characteristic. Beam is also extracted from stationary buckets at a phase angle which would be at the upper tip of the characteristic because we are above transition. Since both of these points are unsuitable from a feedback standpoint it is necessary to compress the characteristic by having unequal delays in the signal paths between the detector, transformer, and cavity gaps. The transformers are offset azmuthally by a quarter of an RF wavelength from the cavity gaps. The cables are then mismatched by approximately 60° using the digitally controlled delay line (PO and TRP) to achieve the desired operating range.

Having covered the functions of the various modules comprising the basic LLRF, we can appreciate an individual detailed description of each one.

REFERENCE SOURCE

This device is basically a precision integrator which may be either clamped to an adjustable dc voltage level necessary to produce the correct value of F_o, or unclamped and programmed to provide a voltage waveform for the VCO.

Binary data representing the $\dot{F}$ program is converted to a current and applied to the input of the integrator as shown in Figure 3. Also an input, is an adjustable current sink of approximately 4.5 mA acting as a $\dot{F}$ zero adjust. Since the $\dot{F}$ program starts with $\dot{F}$ being zero, the adjustment balances the initial current input from the $\dot{F}$ D-A converter preventing drift when the integrator is first unclamped.

When clamped, the integrator output voltage is compared to a design value. The difference between the two is compared with a D-A converter voltage (F_o) which represents a correction to the design value. The result is amplified by a limiting amplifier and gated back to the integrator to maintain its output at the correct rest frequency prior to the start of the frequency sweep. As soon as the clamp command is given, the voltage present at the output of the limiting amplifier is gated into the integrator to drive its output back to the starting or rest value.

Two FET switches are used in the clamp circuit with drivers to interface them to input TTL logic levels. The stored charge in the switches is compensated to a negligible level to produce transient free switching. In addition, a maximum unclamp time of 40 msec is provided by an internal one-shot.

VCO

The VCO employed here is a modified Hartley oscillator which is tuned over a small range by means of voltage variable capacitors, see Figure 4. The frequency of this oscillator is swept between 240 MHz and 263 MHz. The output is

split into two isolated channels having greater than 80 db isolation. Each VCO channel is then heterodyned with a crystal oscillator to provide the correct output frequency. The 30 - 53 MHz sweep employs a crystal frequency of 210 MHz, and the 40 - 63 MHz sweep employs a 200 MHz crystal. The reason for high-isolation between the 30 - 53 MHz and 40 - 63 MHz sources is to minimize spurious output caused by 30 - 53 MHz RF in the 40 - 63 MHz local oscillator. The VCO is located in the same physical module as the reference source and for practical purposes, may be considered as one unit.

DRIVER AMPLIFIERS

Two of these amplifiers are used to bring the signal level of each VCO output channel up to a constant level of 900 mV p-p across 50 ohms. The constant output level is achieved by the use of an automatic gain control (AGC) circuit. Each amplifier also employs an appropriate band-pass filter to remove high order harmonics in the VCO output waveform. The gain of the input stage may be changed 10 to 20 dB by shifting the bias current through a diode in the emitter circuit. The output RF level is detected and compared to an adjustable reference level to provide an AGC correction voltage that is used to generate the required bias through the gain control diode for AGC action. The output level can be held flat to better than 0.5 dB during the frequency sweep. Both driver amplifiers are contained in one module.

PHASE DETECTOR

Both the swept RF signals representing the beam current and the cavity gap voltage are mixed with the 40 - 60 MHz "local oscillator" from the VCO. This results in two 10 MHz signals which have amplitudes proportional to the swept inputs and maintain the same phase relation as their swept counterparts. This is shown in Figure 5. The 10 MHz intermediate frequency ω' is extracted through a bandpass filter in each channel, and then limited to provide constant amplitude signals whose phase difference is proportional to the beam-cavity gap phase. A dc voltage proportional to this phase difference is provided by a conventional 4-diode phase detector. The phase detector is designed to handle beam currents from 1-2 mA up to 250 mA without external attenuators with the conversion gain being 12 mV/Deg.

DELAY LINE

To provide remote adjustment of the line length between the beam current transformer and the phase detector, a digitally adjustable delay line is provided. Within the device, any combination of eight delay cables cut in binary lengths may be connected in series or bypassed by means of solid state switches. This is shown in Figure 6a. The length of the most significant delay is $\lambda/2$ at 50 MHz which corresponds to a time delay of 20 nsec. A typical switch section is shown in Figure 6b. The TTL input is complemented to provide the differential control necessary to activate either side of the differential amplifier. The resulting level shift forward biases the appropriate diode on the input of either the delay cable or the bypass. The switched differential amplifier employs matched pairs of transistors and serves to isolate the cable sections. This system has a characteristic impedance of 90 ohms, and a resolution of approximately 1.4 degrees. This device shares a module with the phase detector.

RADIAL POSITION DETECTORS

Two RF voltages are derived from each beam position transformer. One is a measure of beam intensity or "sum" (Σ). The other is a measure of the position of the beam relative to the center of the opening of the position transformer. This difference signal (Δ) changes sign or phase relative to the Σ depending upon whether the beam position is to the right or left of center. The detectors must develop voltages proportional to the amplitude of both signals, and provide the proper polarity for the Δ input.

As was the case for the phase detector, both swept inputs are heterodyned to a fixed 10 MHz carrier. The carrier which represents the Σ input is split into two independent channels, one of which is limited, and the other delayed by an amount equal to the transit time through the limiter. The limiter output which serves as the reference and the delayed output (both of which are in phase) are compared in a balanced mixer. The result is a dc voltage which is proportional to the non-limited input or Σ input. This technique is known as "synchronous detection". The carrier which represents the Δ input is delayed by an amount equal to the transit time through the Σ reference channel (transit

time through the limiter and the power splitter). This voltage is also compared with the limiter output to produce a dc voltage proportional to the Δ input.

Two independent detectors are used, one for each position transformer; their respective dc sum and difference voltages are combined to provide a more representative picture of the average position. The composite sum is used in the control room as a measure of beam intensity.

NORMALIZING

The magnitude of the difference voltage is proportional to beam intensity, and for it to become a useful measure of position, this effect must be removed. Useful position data can be acquired by dividing the difference voltage by the sum voltage. This division is referred to as "normalizing". Historically, the normalizing was done with a separate device; but with the commercially available high precision division modules, this process becomes trivial from a technical standpoint.

BEAM FEEDBACK

This portion of the system can be considered the "nerve center" of the LLRF for it is here that signals from the phase measuring system, the position measuring system, and the booster to main-ring synchronizing system are combined in such a manner as to provide a correction voltage to the VCO so that its output frequency remains "locked" to the frequency of the circulating bunches as acceleration progresses. Under beam control, only one dc coupled feedback loop is used - radial position. With reference to Figure 8, it can be seen that the normalized radial position voltage is compared to a position reference voltage. The position reference voltage generator converts a string of digital words into the desired reference waveform. The transition from one value to the next is done with a constant slope. This transition slope may be adjusted from the front panel to fix the maximum desired dR/dt. An auxiliary input is provided on the reference generator to accept errors from the gap rotation system (future). The

difference between the reference position and the actual position goes through a sign changing amplifier. This provides the required sign change in the radial feedback error signal at transition. The sign change is initiated by a pulse at transition (TRT) and reset at the beginning of the acceleration cycle with T_0. From the sign changing amplifier the error voltage goes to the digital gain control. This gain control is simply an analog multiplier with the error voltage as one input, and the output of the R-Gain D-A converter as the other. Data into the D-A converter may be logically enabled or inhibited by external logic commands. One such input enables the data to be transmitted to the D-A as long as the beam intensity exceeds some threshold. A second input turns the gain off (all bits zero) when the booster RF is phase locked to the main ring prior to extraction. The error voltage is then processed by a frequency compensating amplifier to provide the desired system response. It is then combined with other correction voltages in a summing amplifier, the output of which provides the feedback correction to the VCO. A second input to the summing amplifier comes directly from the booster - main ring phase lock. No gain control is provided for this input.

The input from the beam-cavity phase detector passes through a high-pass filter with cutoff set at 300 Hz. The filter removes the dc or synchronous component from the phase detector output. The resulting signal is a measure of the transient motion between cavity and beam. This voltage is operated on by a digital gain control similar to that used in the radial control loop. It is then summed with the other correction voltages where it serves to damp coherent phase motion of the beam during acceleration.

SYNCHRONIZATION WITH THE MAIN RING

Beam from successive cycles of the booster is stacked end to end in the main ring. Beam previously injected into the main ring is held in stationary RF buckets. To capture beam from subsequent booster cycles, the phase and frequency of the beam bunches in the booster are locked to the frequency of the main ring system before beam is transferred. Prior to extraction, the booster radius is

programmed to the inside. Since it is operating above transition, its frequency will match that of the main ring several msec before extraction. At this point, the control of the booster frequency is determined by the main-ring frequency via the phase-lock system instead of radial feedback. With its revolution frequency fixed, the beam sweeps outward with the rising magnetic field. When the field has reached the 8-GeV value, beam is extracted.

PHASE LOCK

The main-ring RF signal is transmitted to the phase-lock module in the booster LLRF system. This phase-lock circuit monitors the instantaneous phase difference between the main-ring RF signal and the RF structure of the beam bunches in the booster. In the diagram of the phase-lock system shown in Figure 9, we see that the phase detector is basically the same as that used to measure beam-cavity phase except that each limited 10 MHz channel has two outputs. One is used for a direct comparison of the phase between the two channels with a balanced 4-diode detector to provide the pattern shown in Figure 10a. A second output from the channel representing the booster RF is delayed by 25 nsec ($\lambda/4$ at 10 MHz) before it triggers a $\div$ 2 counter. The second output from the channel representing the main-ring RF also triggers a $\div$ 2 counter. The outputs of these two counters is also compared in phase with the result shown in Figure 10c. Zero crossing detectors monitor the two phase detector outputs to generate the logic levels shown in Figures 10b and 10d. These logic levels provide data for circuits which must indicate the slope of the phase-voltage characteristic (Figure 10e) and which synchronize the start of phase lock π radians before the beam is aligned with the empty buckets. The second phase detector (which compares the two counter outputs) has an output which goes through zero each time the booster beam and main-ring buckets are aligned. It, therefore, can be used to generate an error signal which can be used to keep these two together. The phase detector output, however, is periodic and changes slope for every 2π radians of phase advance. For this reason, the phase-lock system must be kept informed as to what the slope of the phase detector characteristic is at any given time so that the proper sign may be applied for negative feedback to the LLRF. The frequency difference between

booster and main ring is monitored by a frequency discriminator which measures the time interval between consecutive zero crossings of the phase detector. When this interval exceeds some value set by the operator (DFE) the discriminator enables the phase lock to begin. The turn-on synchronization logic is armed by the SYEN pulse which usually occurs around transition. The reason for this is to prevent a zero beat which occurs when the booster RF structure is 20 MHz (twice the intermediate frequency of the phase detector) below the main-ring RF.

At the onset of phase lock, the ouput of the second phase detector is held to serve as the initial value for a "model" to which we would like the phase to conform during its transition to zero. The hold circuit is modified to decay at an expotential rate with the time constant adjusted to provide a match to $d\phi/dt$ at the start of phase lock. The model and the phase detector are compared to provide an error voltage. The appropriate sign is given to this error by the polarity select logic and the result is gated into the LLRF feedback module. The transition is quite smooth since intially the module and the phase detector have the same value and no error voltage has developed.

TIMING SEQUENCE

The booster extraction system and main-ring injection system must be synchronized with a reference point on the main-ring circumference which indicates where beam is to be placed. A marker pulse is generated by counting cycles of the main-ring rf voltage and scaling by the harmonic number (1113). The result is a pulse train occuring at the main-ring revolution frequency. When transfer time is reached in the booster cycle, a pulse (TEXTR) from the booster clock enables the timing sequencer to synchronize with the main-ring marker pulses. This system is shown in Figure 11. The timing sequencer is simply a 10-stage shift register which is clocked with the main-ring marker generator. This gives very precise delays in increments of the main-ring revolution frequency. Smaller delays are achieved through "one-shot" multivibrators. The timing sequence for beam transfer is shown in Figure 12. After each extraction sequence, the main-ring RF to the ÷ 1113 counter is turned off

for approximately 1.6 μsec. This delays all future marker pulses by the length of one booster batch, therefore each new batch will fall directly behind the last batch.

Additional circuitry has been included in this module for "cogging" the booster which is part of the process for synchronizing a 3-bunch gap in the booster beam with the firing of the kicker magnets. At the present time, it has been disabled to stop the ±42 usec pulse-to-pulse jitter in extraction timing caused by the cogging process.

EQUIPMENT LAYOUT

The LLRF equipment resides quietly in an RFI shielded rack at the north end of the East Gallery. This location was chosen to provide the shortest transit time through the beam feedback loops for optimum system response.

The high sensitivity of the beam sensing electronics requires a high degree of shielding on all signal inputs and outputs. RF signals into and out of the rack are transmitted through rigid coaxial cables decoupled from the source (or destination) by toroidal chokes. Data which is digital in nature is coupled through either differential line receivers or optical isolators. The net result is that all signal conditioning electronics is in an electrically "clean" environment.

Three main frames house the twelve modules which comprise the two LLRF systems and the synchronization electronics. These main frames contain temperature control equipment and air recirculation systems to maintain the modules at a constant temperature.

Both the 40 - 63 MHz and the 30 - 53 MHz outputs from the LLRF which has been switched on line are amplified to a power level of 2 watts into 50 ohms. For this purpose, two ENI wide-band amplifiers are used.

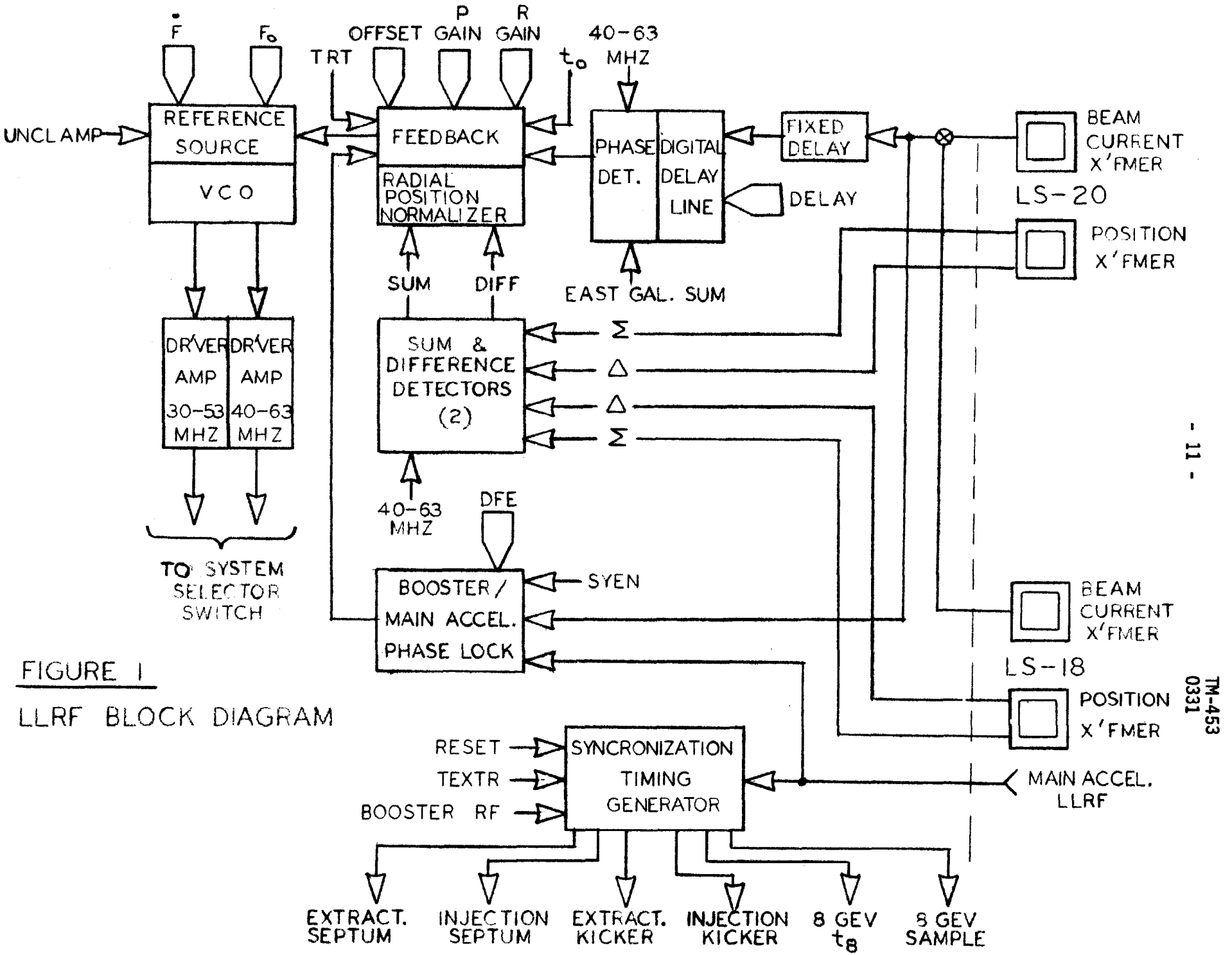

FIGURE 1

LLRF BLOCK DIAGRAM

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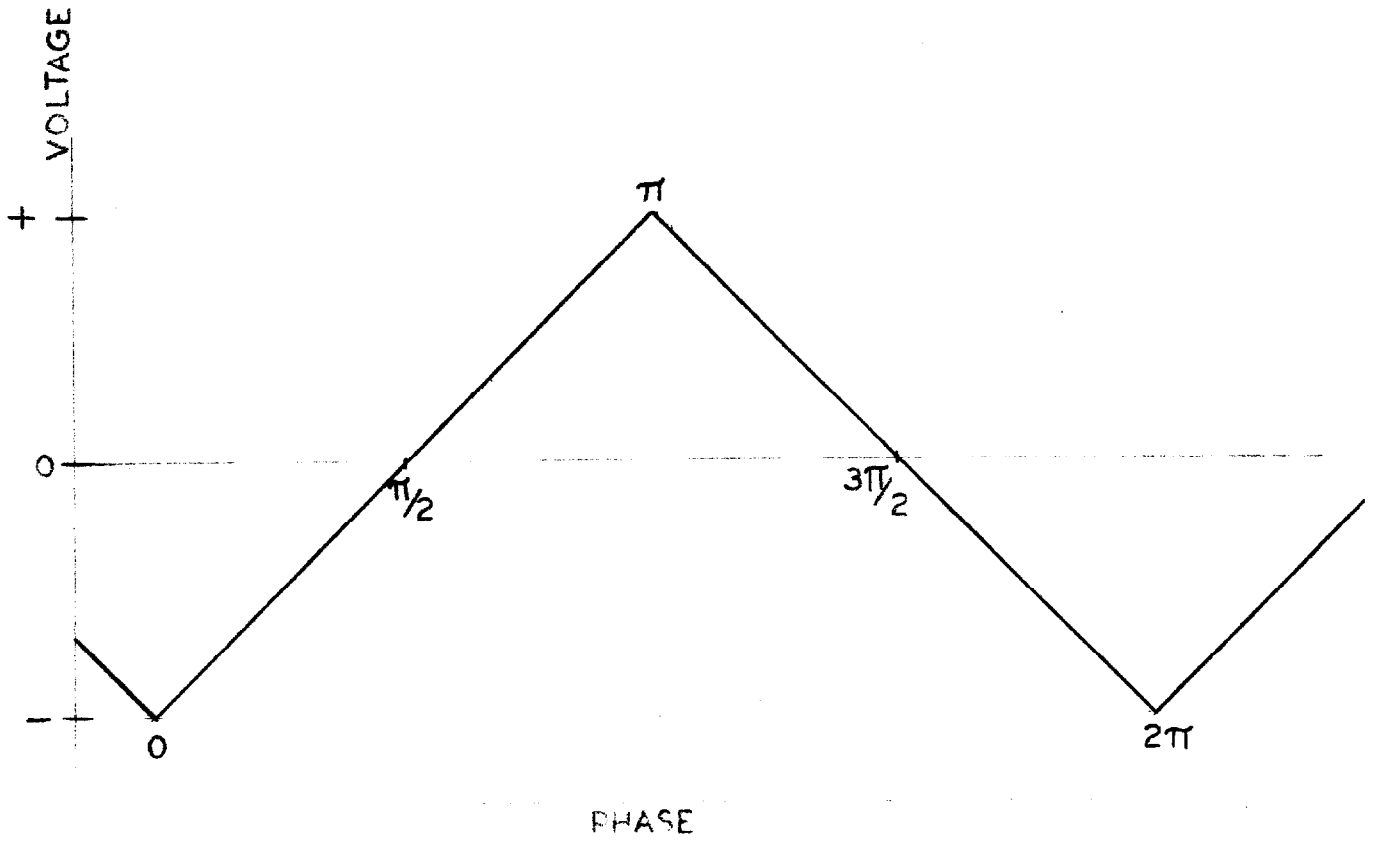

FIGURE 2

PHASE DETECTOR – VOLTAGE TO PHASE CHARACTERISTIC

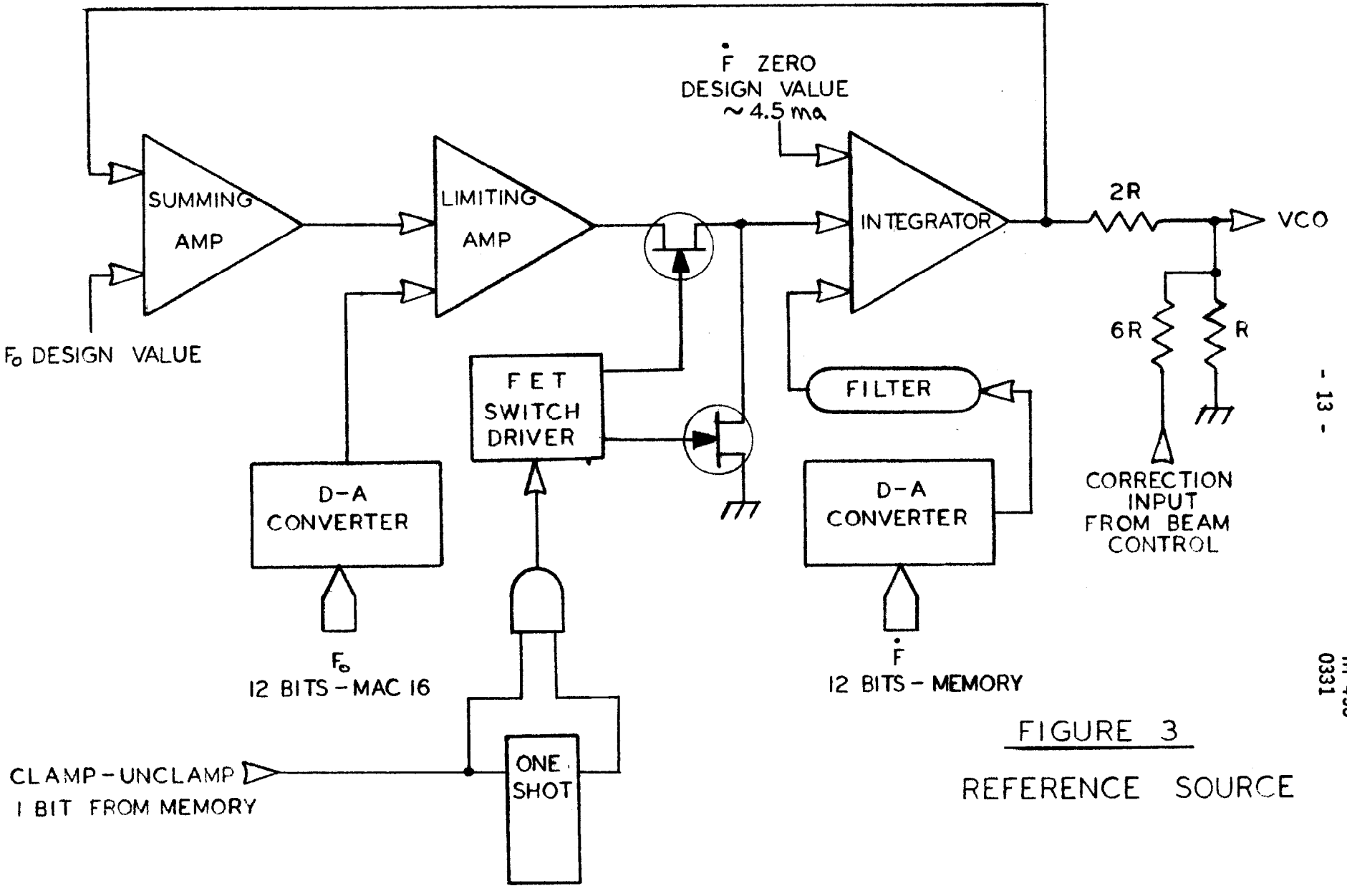

FIGURE 3

REFERENCE SOURCE

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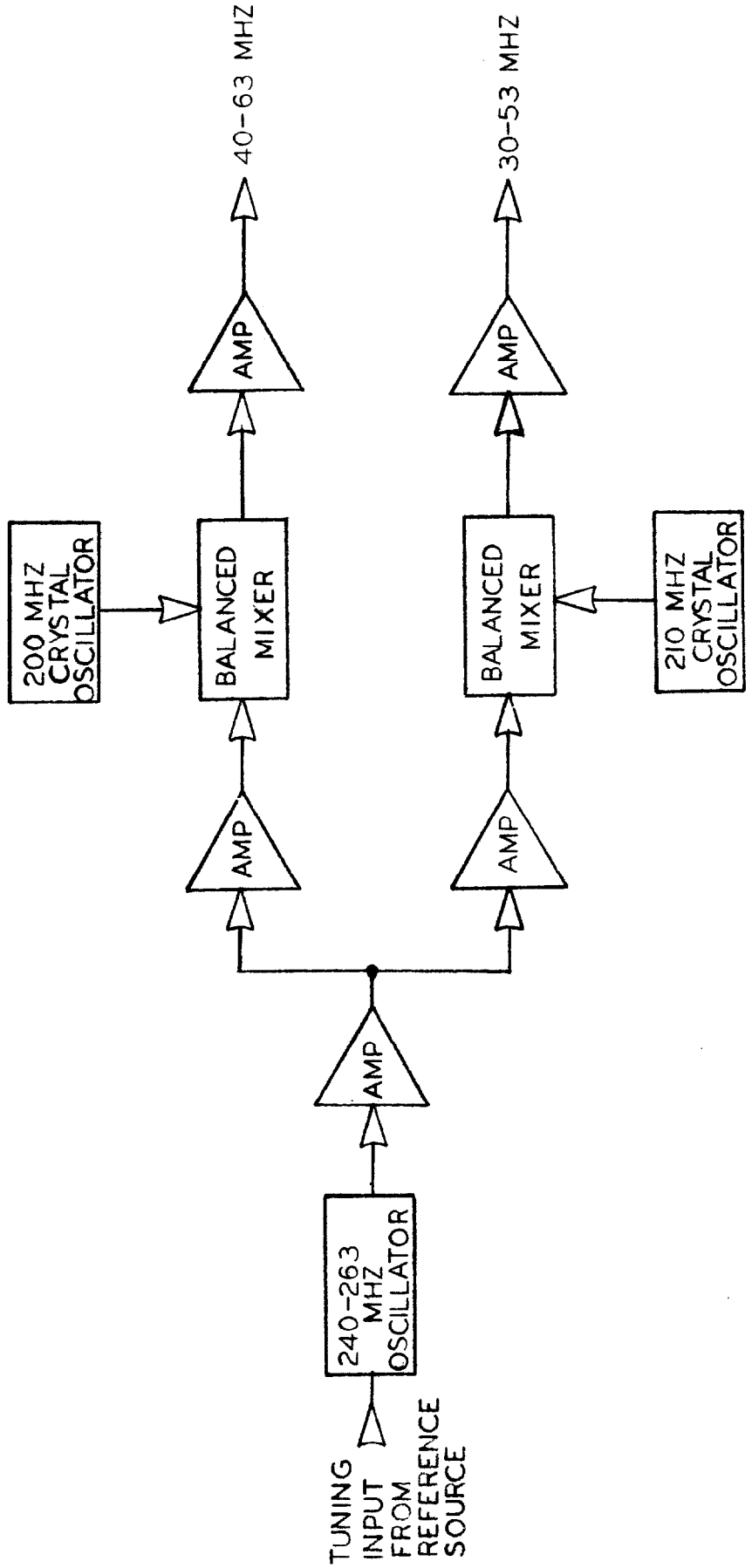

FIGURE 4 VOLTAGE CONTROLLED OSCILLATOR

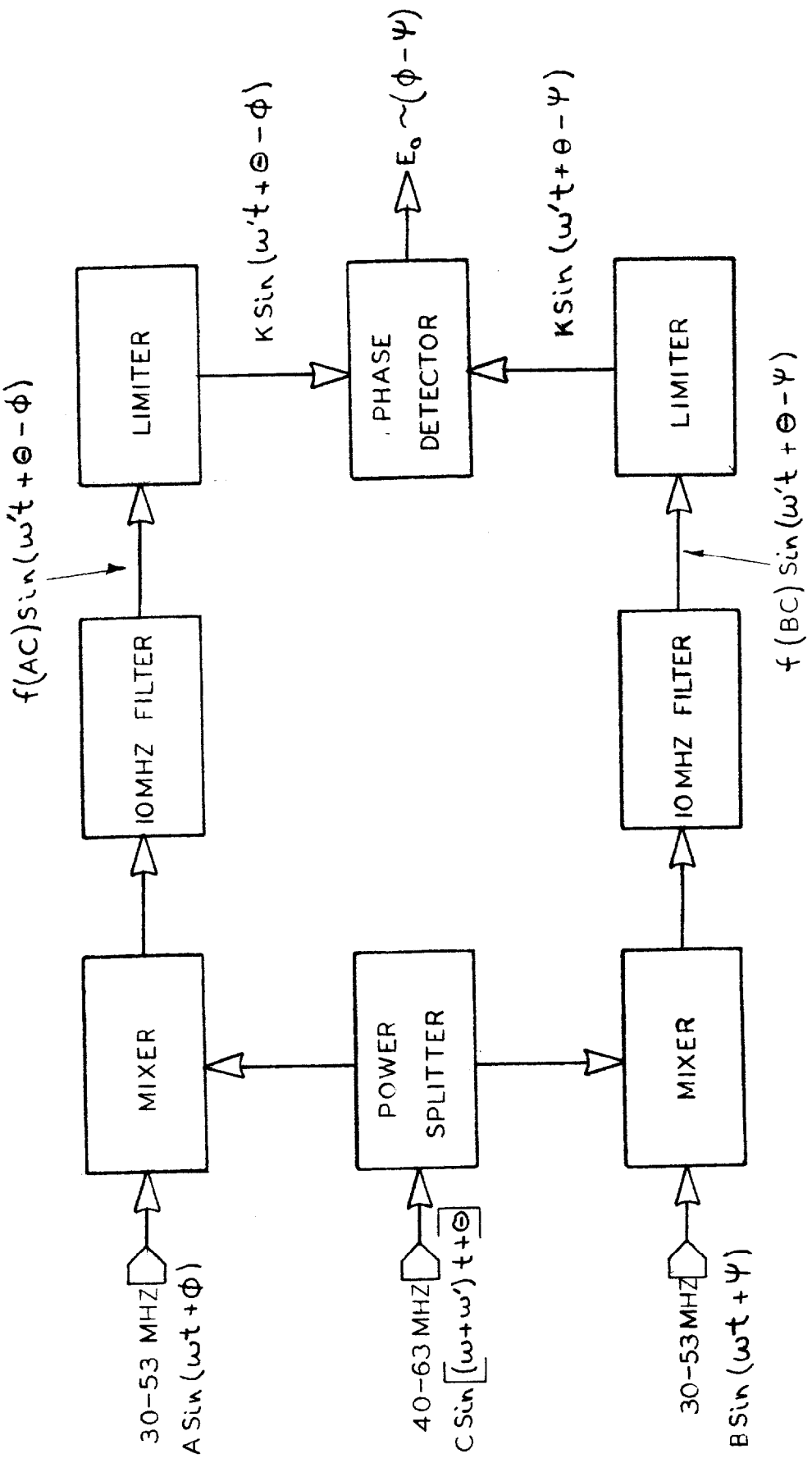

FIGURE 5 PHASE DETECTOR

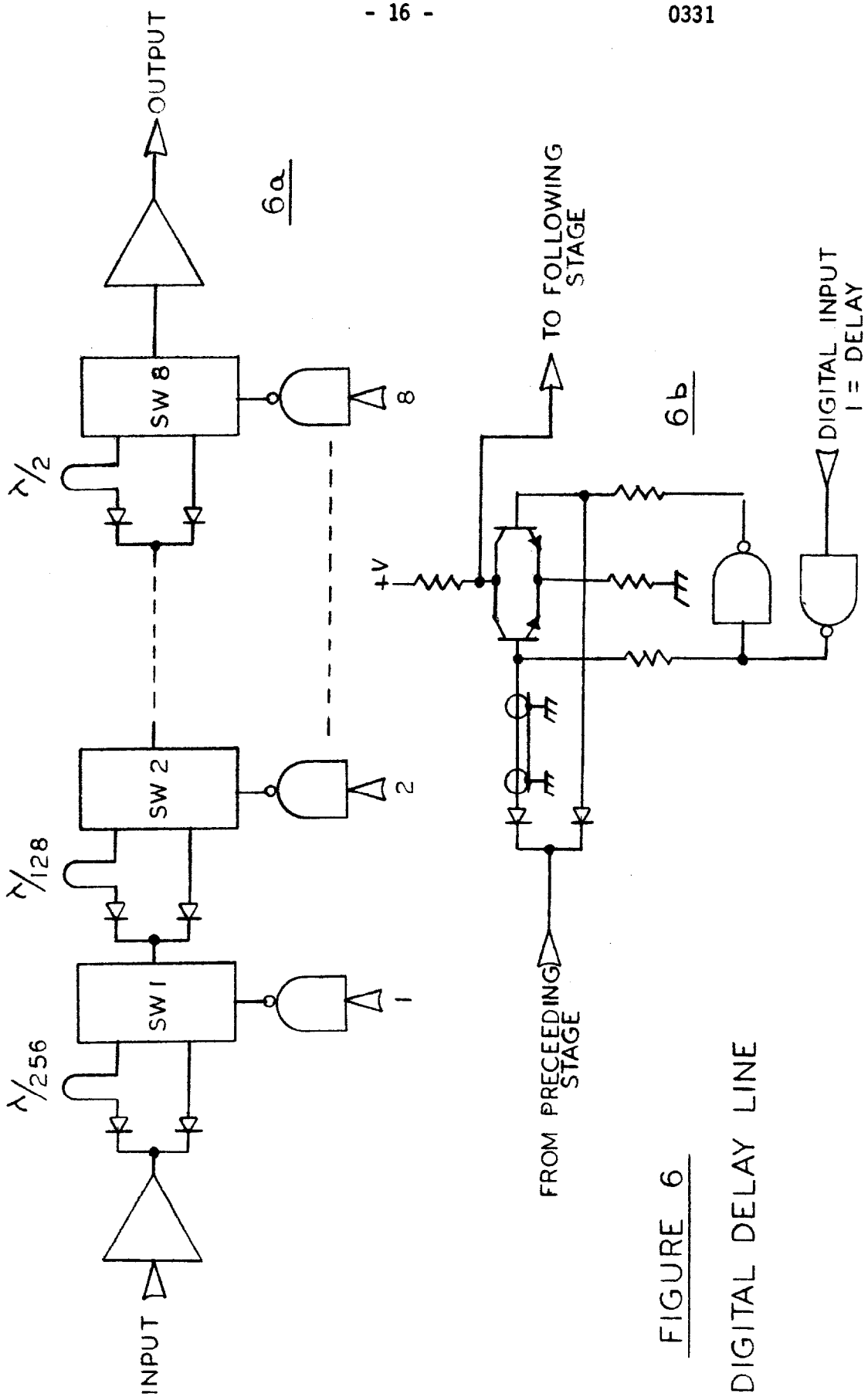

FIGURE 6

DIGITAL DELAY LINE

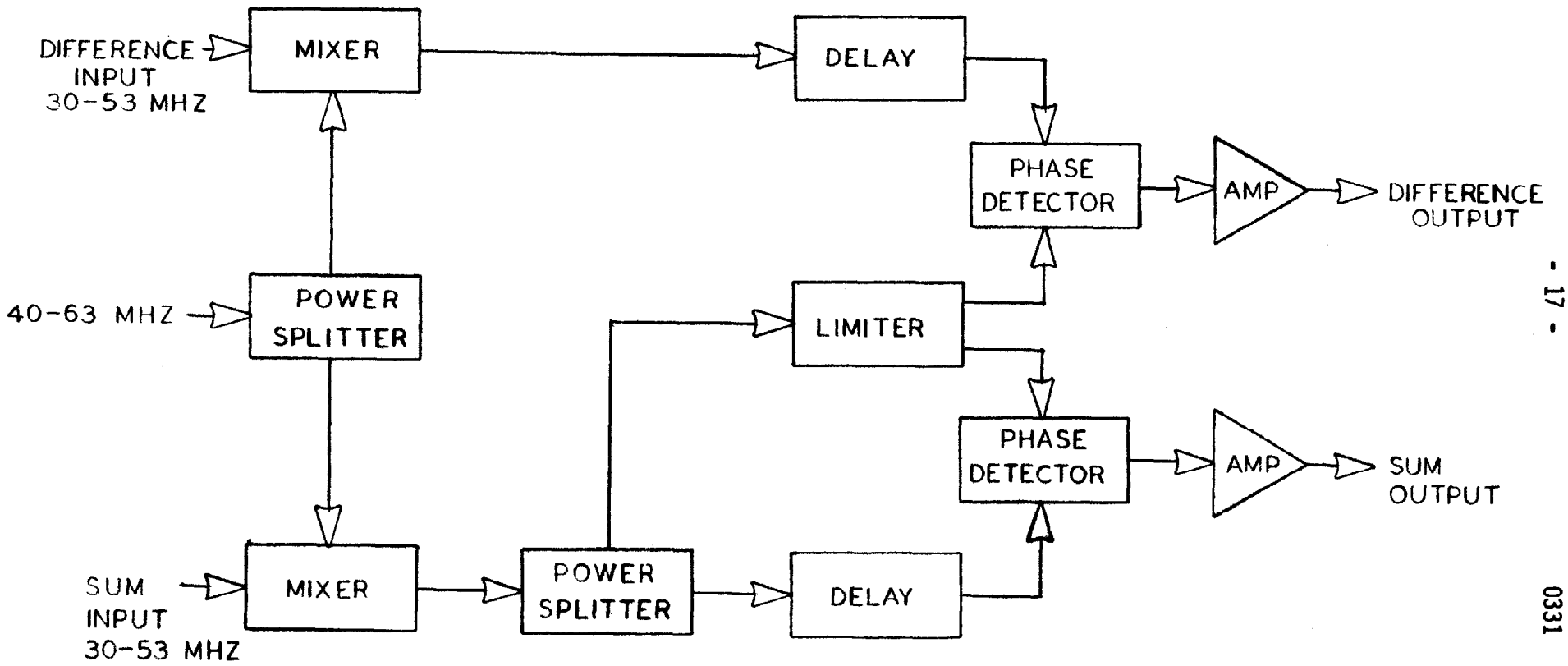

FIGURE 7

RADIAL POSITION SUM & DIFFERENCE DETECTOR

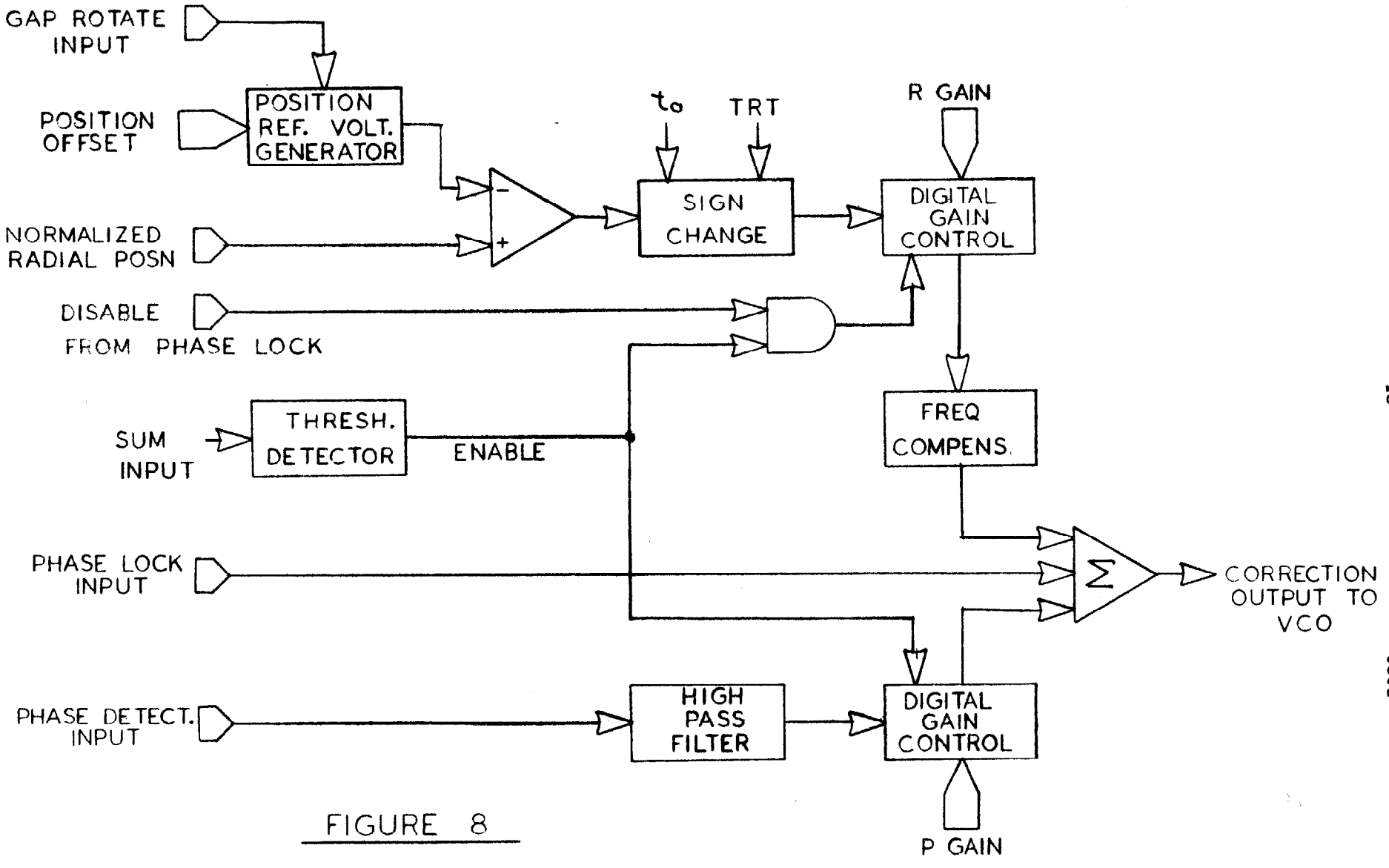

FIGURE 8

BEAM FEEDBACK CONTROLLER

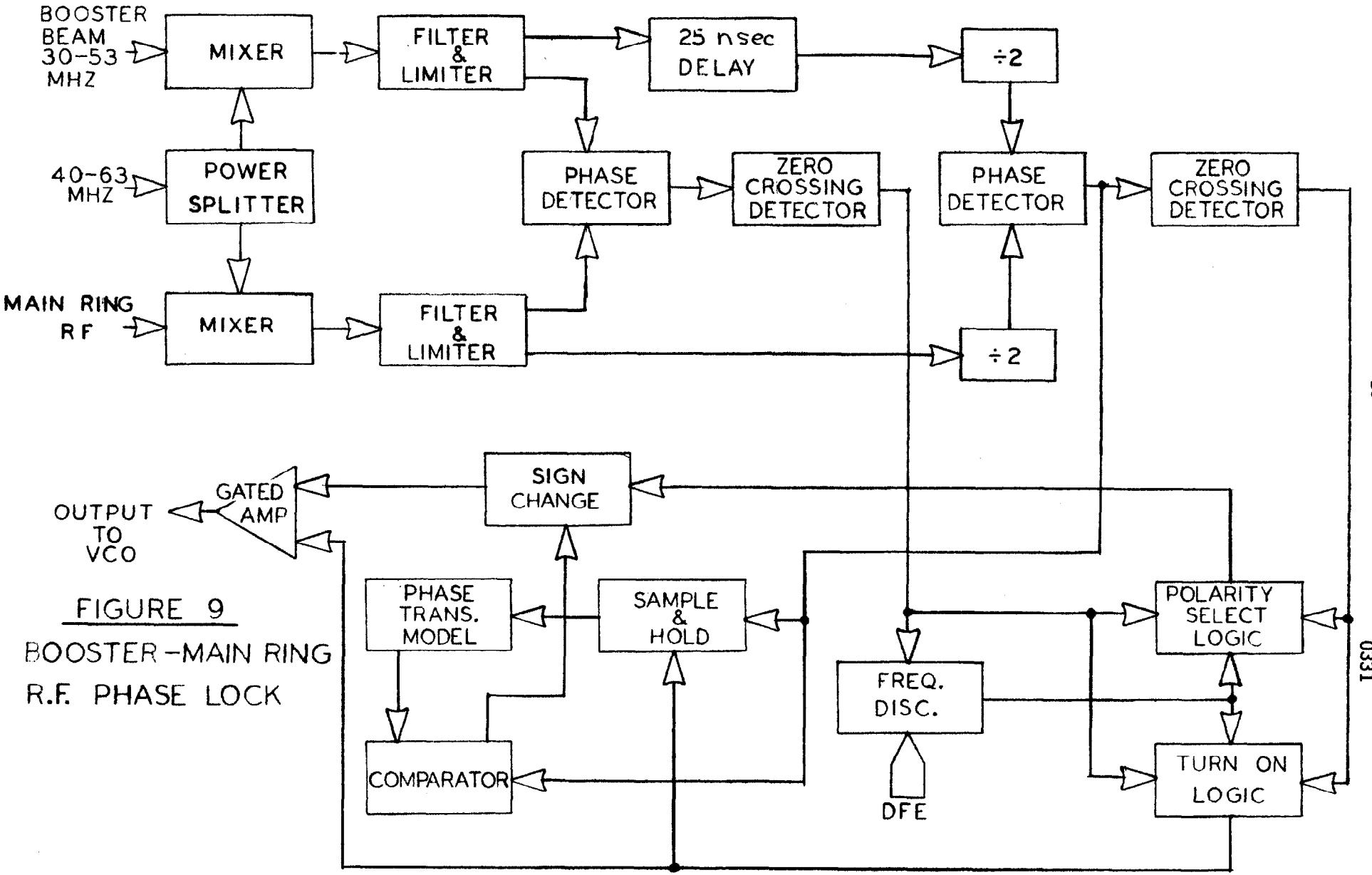

FIGURE 9

BOOSTER-MAIN RING R.F. PHASE LOCK

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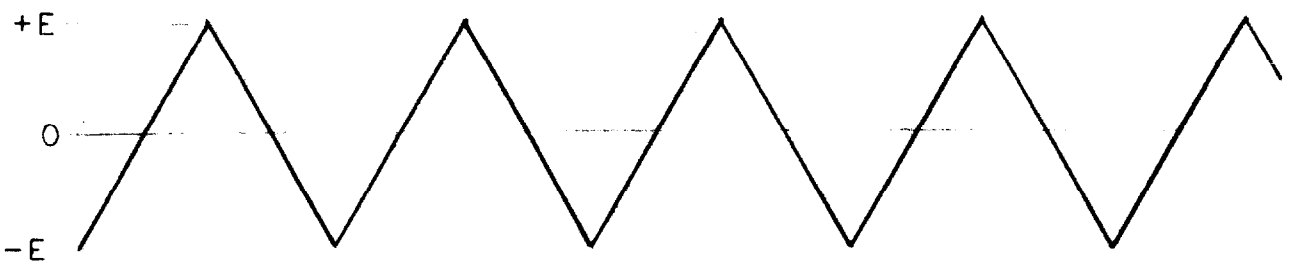
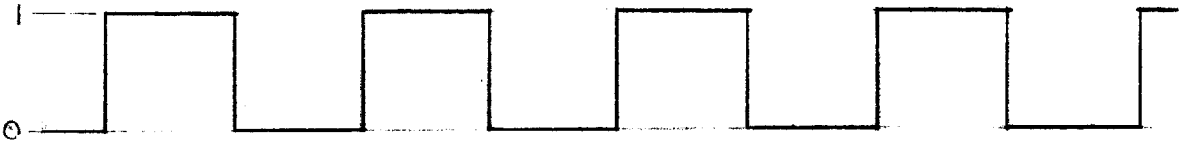


10 A



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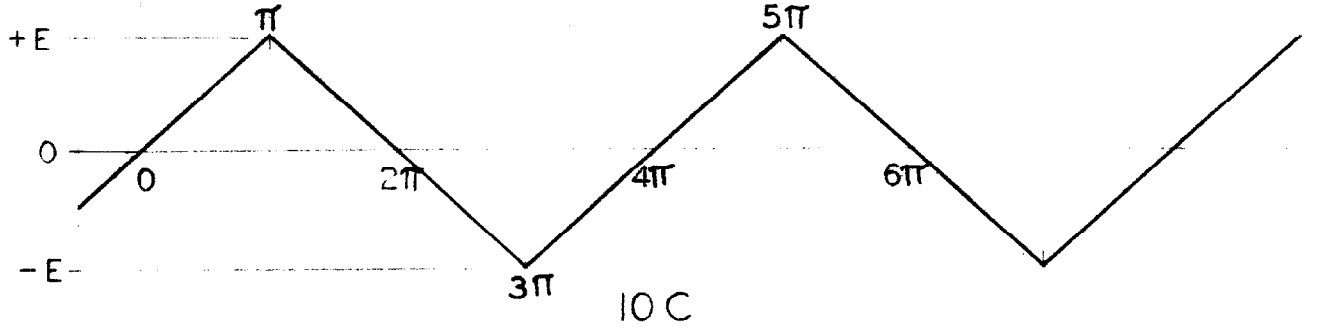

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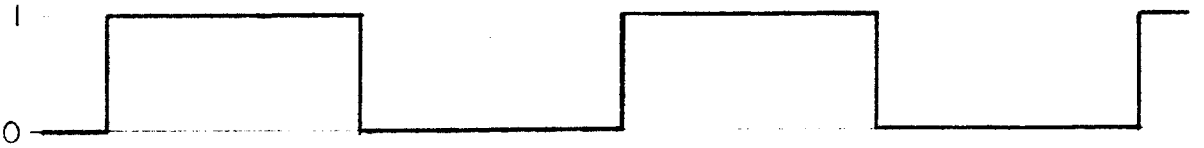

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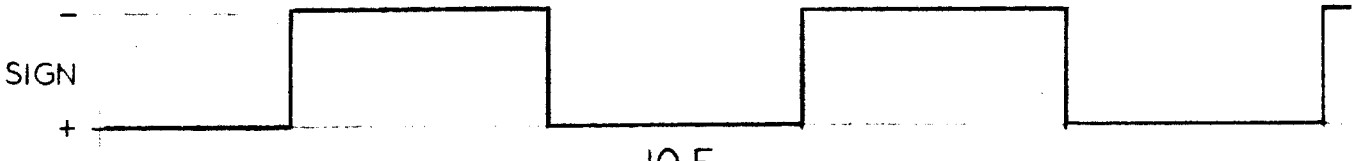

10 E

FIGURE 10

BOOSTER – MAIN RING PHASELOCK WAVEFORMS

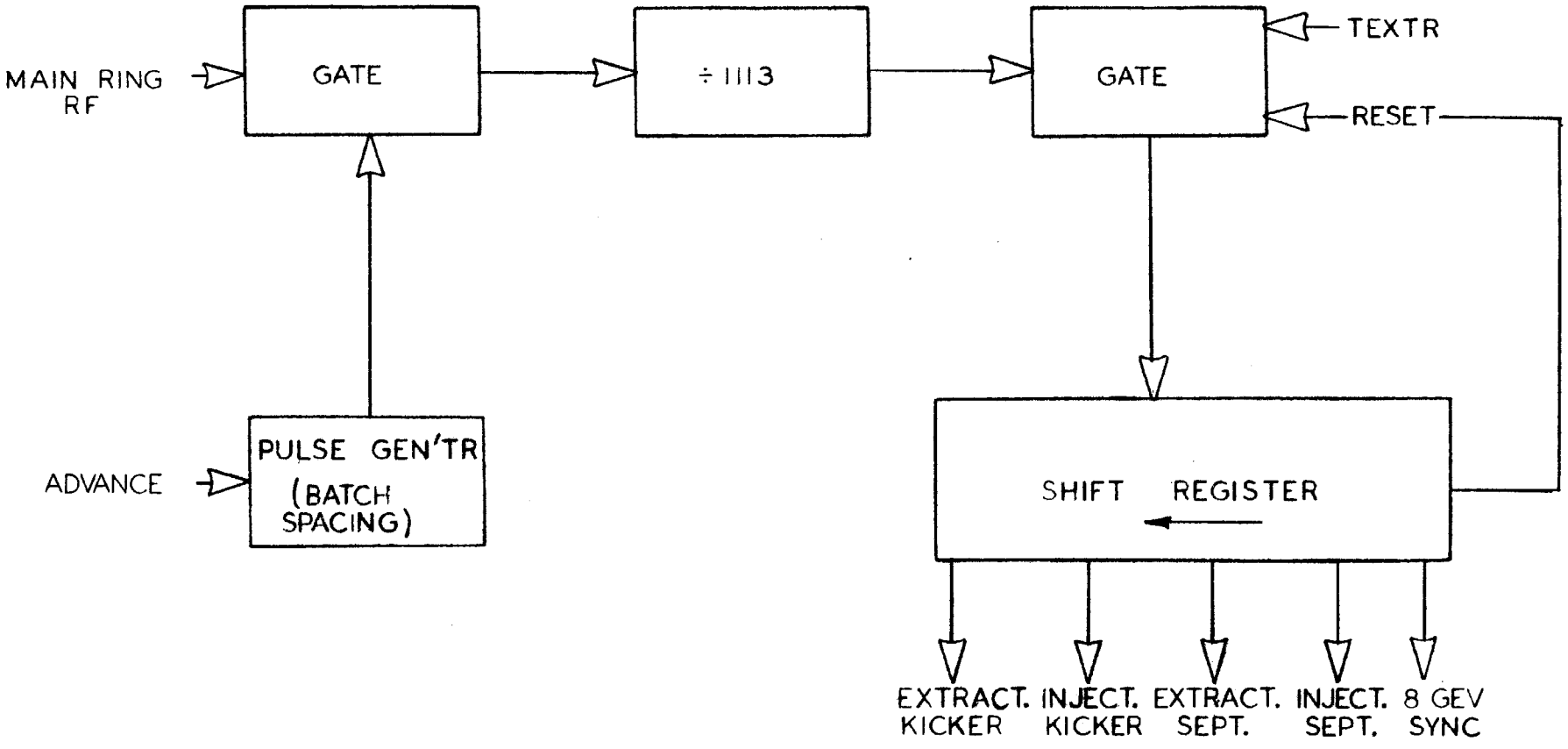

FIGURE 11 SYNCRONIZATION TIMING MODULE

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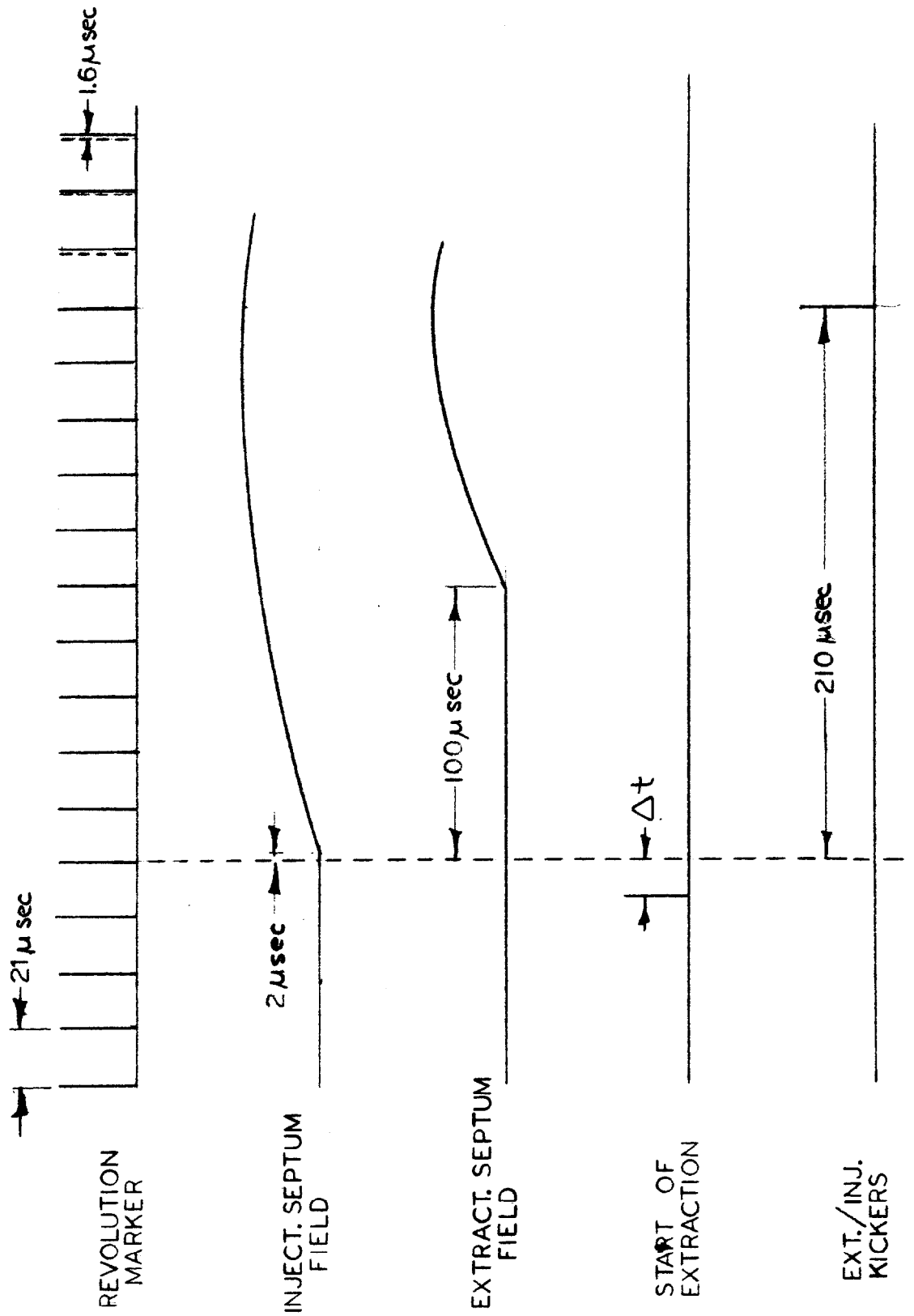

FIGURE 12

BEAM TRANSFER TIMING FOR MULTIPLE PULSE INJECTION